Fortior Tech

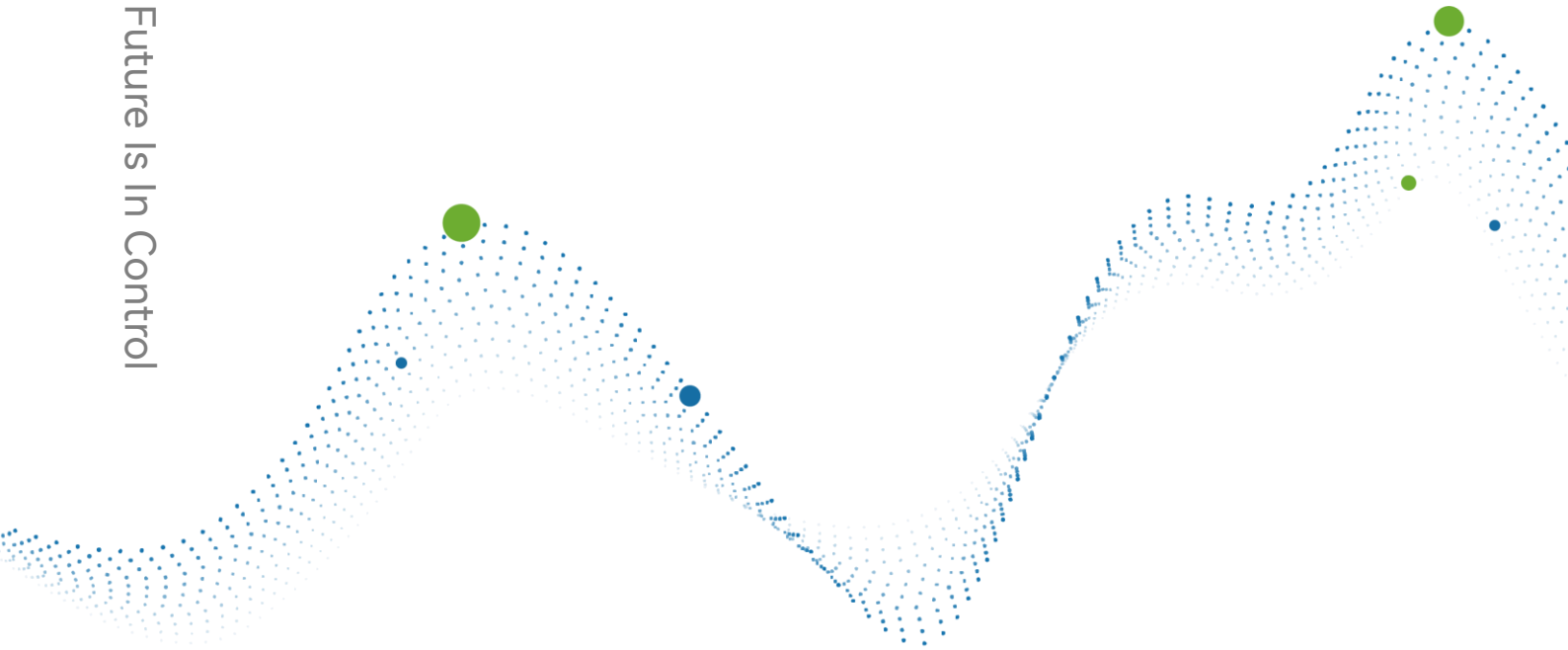
DATASHEET

FD2161S

100V Three-phase Gate Driver

Preliminary

Future Is In Control



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Preliminary information: The product is in design and development. The datasheet represents the product as it is understood but details may change.

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Contents

1 System Introduction

1.1 Overview

FD2161S is an integrated circuit (IC) that integrates three independent half-bridge gate drivers. It is specially designed for high-voltage and high-speed MOSFET driver applications.

FD2161S supports VBB/VBS under-voltage lockout (UVLO) feature, protecting the power tube from operating with insufficient voltage.

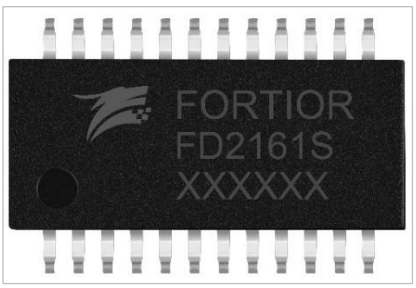
5V/30mA LDO and 12V/30mA LDO supply power for MCU or others.

FD2161S also provides cross-conduction prevention and deadtime insertion to effectively protect the power IC and prevent both MOSFETs of each half-bridge from switching on at the same time.

1.2 Applications

- Power tools

Figure 1-1 FD2161S

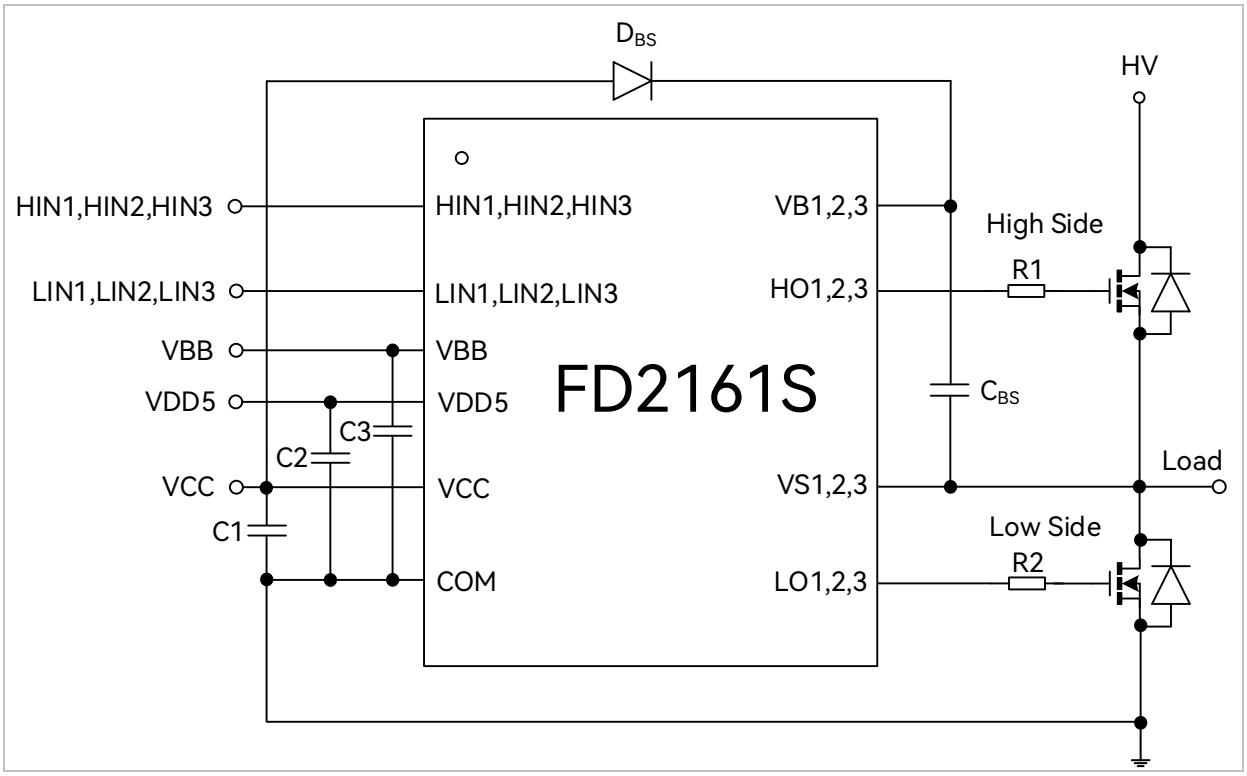


1.3 Features

- Fully operational to +100V
- Power supply: 4.4V ~ 20V
- Output current: +0.6A/-0.6A
- Three independent half-bridge drivers
- 3.3V/5V logic input compatible
- VBB/VBS under-voltage lockout (UVLO)
- Integrated 5V LDO and 12V LDO
- Cross-conduction prevention logic
- Built-in deadtime module
- Inputs in phase with outputs

1.4 Typical Application Diagram

Figure 1-2 Typical Application Diagram



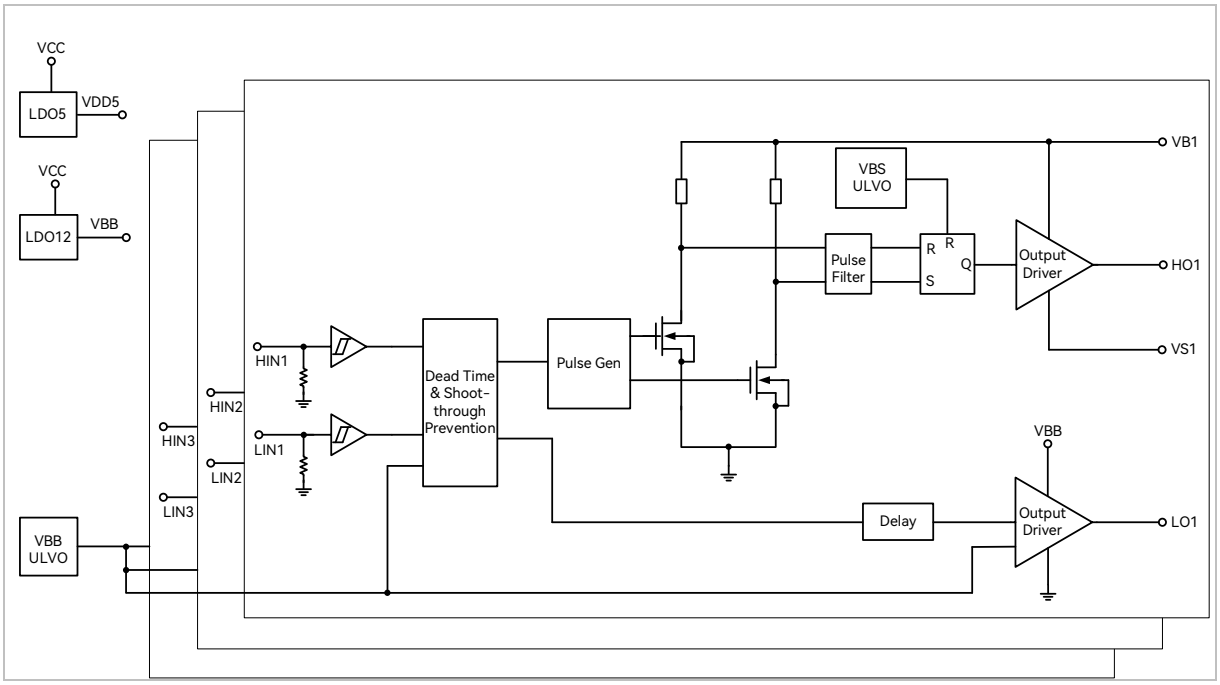
- C1: 10μF ~ 100μF power filter capacitor depending on the application circuit.
- C2 and C3: 10μF ~ 100μF power filter capacitor depending on the application circuit.
- R1 and R3: Gate drive resistor. The resistance depends on deadtime and the device being driven.
- DBS: Bootstrap diode. Those with high reverse breakdown voltage and short recovery time are preferred.
- CBS: Bootstrap capacitor. 1μF ~ 100μF ceramic capacitor or tantalum capacitor is preferred.

Note:

The above circuit and parameters are for reference only. The actual circuit shall be designed with the measured results.

1.5 Functional Block Diagram

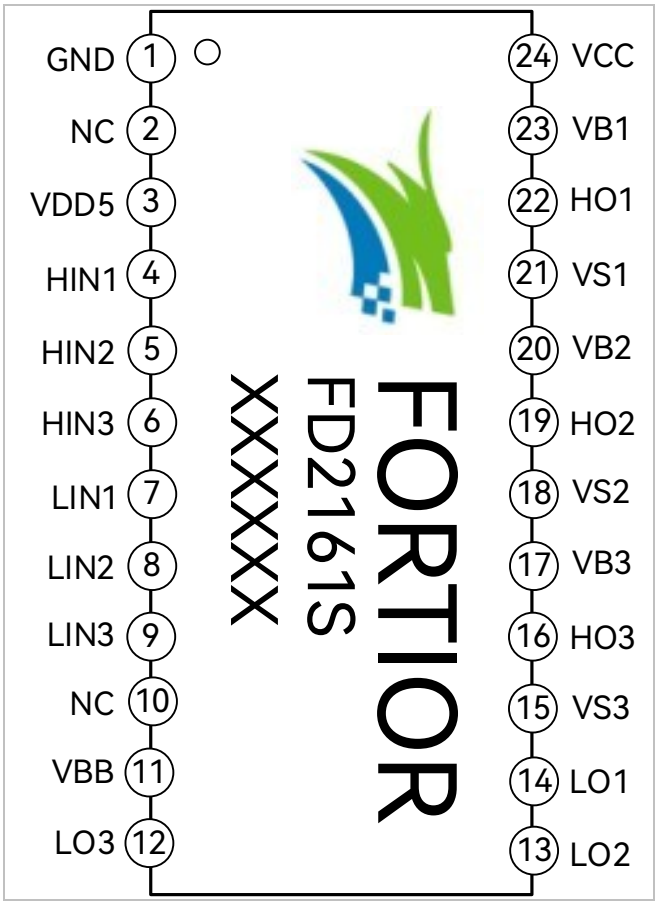
Figure 1-3 Functional Block Diagram of FD2161S



1.6 Pin Definitions

1.6.1 FD2161S SSOP24

Figure 1-4 FD2161S SSOP24 Pinout Diagram



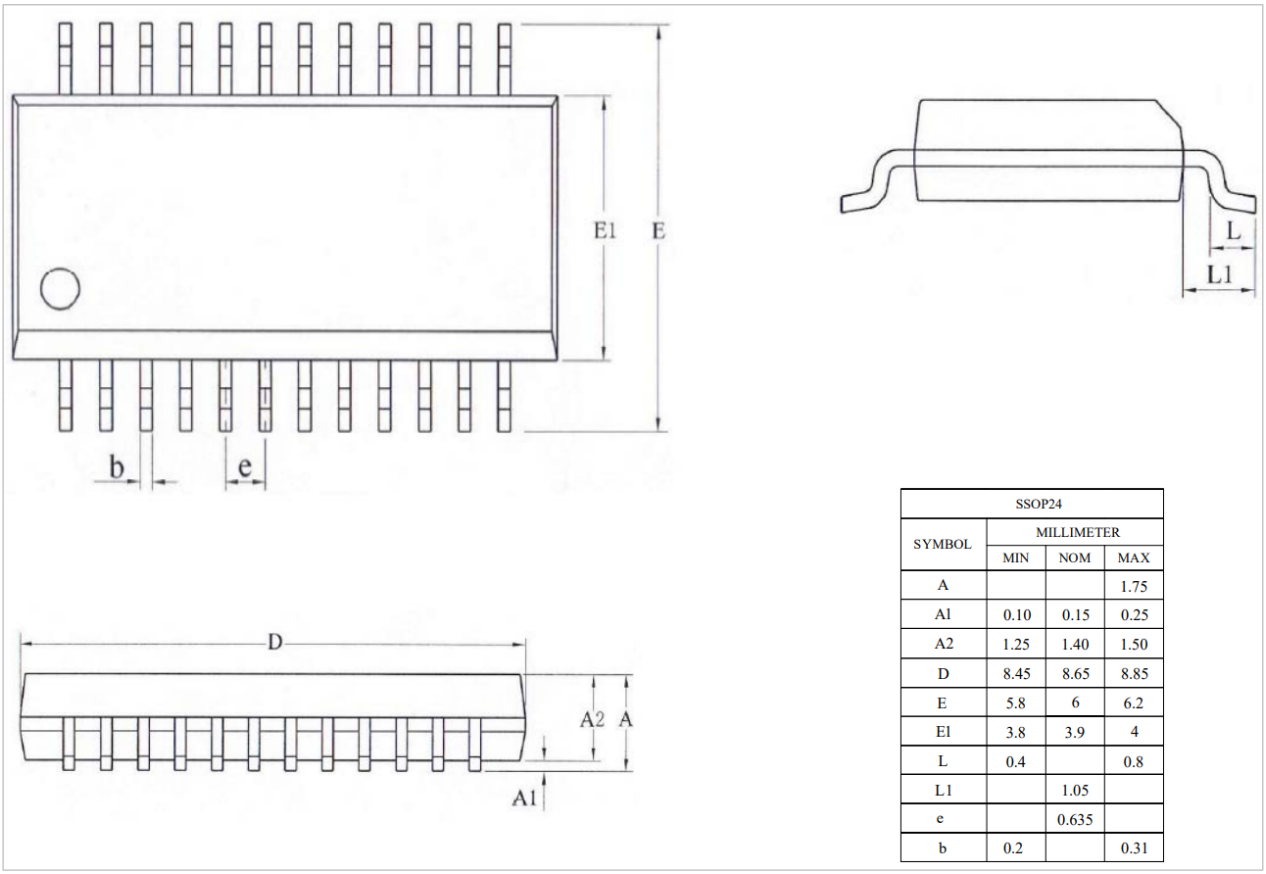
1.6.2 FD2161S SSOP24 Pins

Table 1-1 FD2161S SSOP24 Pins

Pin	FD2161S SSOP24	Function Descriptions
GND	1	Power ground
Not connected	2,10	Not connected
VDD5	3	LDO 5V output
HIN1,HIN2,HIN3	4,5,6	High-side Input
LIN1,LIN2,LIN3	7,8,9	Low-side Input
VBB	11	LDO 12V output
LO3,LO2,LO1	12,13,14	Low-side output
VS3,VS2,VS1	15,18,21	High-side Floating Offset Voltage
HO3,HO2,HO1	16,19,22	High-side output
VB3,VB2,VB1	17,20,23	High-side Floating Absolute Voltage
VCC	24	Low-side supply voltage

2 Package Information

Figure 2-1 FD2161S SSOP24_3.9x8.65 Package Drawings and Dimensions



SSOP24			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A			1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.50
D	8.45	8.65	8.85
E	5.8	6	6.2
E1	3.8	3.9	4
L	0.4		0.8
L1		1.05	
e		0.635	
b	0.2		0.31

3 Ordering Information

Table 3-1 Ordering Information of FD2161S

Product Number	Package Type	Marking ID	Package Method	Quantity
FD2161S	SSOP24_3.9x8.65 (mm)	FD2161S	Tape&Reel	2000

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

(All pins are referenced to COM unless otherwise specified)

Parameter	Symbol	Range	Unit
High-side Floating Absolute Voltage	$V_{B1,2,3}$	-0.3 ~ 120	V
High-side Floating Offset Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$ – 14 ~ $V_{B1,2,3}$ + 0.3	V
High-side Output Voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$ - 0.3 ~ $V_{B1,2,3}$ + 0.3	V
Low-side supply voltage	V_{CC}	-0.3 ~ 22	V
Low-side Output Voltage	$V_{LO1,2,3}$	-0.3 ~ V_{CC} + 0.3	V
Logic Input Voltage (HIN, LIN)	V_{IN}	-0.3 ~ 6.5	V
Slew Rate of Offset Voltage	dV_S/dt	≤ 50	V/ns
Power Dissipation @ TA ≤ 25C°	P_D	≤ 1.25	W
Junction-to-ambient Thermal Resistance	R_{thJA}	≤ 100	°C/W
Junction Temperature	TJ	≤ 150	°C
Storage Temperature	T_{STG}	-55 ~ 150	°C

Notes:

- In any case, power dissipation shall not exceed PD.
- The chip may get damaged if it operates at voltages exceeding those listed above.

4.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

(All pins are referenced to COM unless otherwise specified)

Parameter	Symbol	Min.	Max.	Unit
High-side Floating Absolute Voltage	$V_{B1,2,3}$	-	100	V
High-side Floating Offset Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$ - 12	$V_{B1,2,3}$ – 4.4	V
High-side Output Voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{B1,2,3}$	V
Low-side supply voltage	V_{CC}	4.4	20	V
Low-side Output Voltage	$V_{LO1,\ 2,\ 3}$	0	V_{CC}	V
Logic Input Voltage (HIN, LIN)	V_{IN}	0	5.5	V
Ambient Temperature	T_A	-40	125	°C

Note:

Exposure to recommended operating conditions for extended periods may affect device reliability. It is NOT recommended to use your device in conditions that go beyond the above stress ratings.

4.3 Power Supply

Table 4-3 Power Supply

(T_A = 25C， VCC = 15V, VBB = VBS1,2,3 = 12V, VS1,2,3 = COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VCC Quiescent Current	I_{QCC}	VIN = 0V or 5V	-	0.22	-	mA
VBS Quiescent Current	I_{QBS}	VIN = 0V or 5V	-	45	-	μA
Leakage Current of Floating Power Supply	I_{LK}	$V_{B1,2,3}$ = $V_{S1,2,3}$ = 100V	-	0.1	5.0	μA

4.4 Input HIN/LIN

Table 4-4 Input HIN/LIN

(T_A = 25C， VCC = 15V, VBB = VBS1,2,3 = 12V, VS1,2,3 = COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High-level Input Threshold Voltage	V_{IH}		-	2.2	-	V
Low-level Input Threshold Voltage	V_{IL}		-	1.5	-	V
LIN High-level Input Bias Current	I_{LIN+}	V_{LIN} = 5V	-	28	-	μA
LIN Low-level Input Bias Current	I_{LIN-}	V_{LIN} = 0V	-	-	1	μA
HIN High-level Input Bias Current	I_{HIN+}	V_{HIN} = 5V	-	28	-	μA
HIN Low-level Input Bias Current	I_{HIN-}	V_{HIN} = 0V	-	-	1	μA
HIN Input Pull-down Resistor	R_{HIN}		-	180	-	kΩ
LIN Input Pull-down Resistor	R_{LIN}		-	180	-	kΩ

4.5 Under-voltage Lockout (UVLO)

Table 4-5 Under-voltage Lockout (UVLO)

(T_A = 25C， VCC = 15V, VBB = VBS1,2,3 = 12V, VS1,2,3 = COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VCC UVLO Lockout Voltage	V_{CCUV+}		-	4.7	-	V
VCC UVLO Release Voltage	V_{CCUV-}		-	4.4	-	V
VCC UVLO Hysteresis Voltage	V_{CCUVH}		-	0.3	-	V
VBS UVLO Lockout Voltage	V_{BSUV+}		-	3.8	-	V
VBS UVLO Release Voltage	V_{BSUV-}		-	3.5	-	V
VBS UVLO Hysteresis Voltage	V_{BSUVH}		-	0.3	-	V

4.6 Static Negative Voltage

Table 4-6 Static Negative Voltage

(T_A = 25C， VCC = 15V, VBB = VBS1,2,3 = 12V, VS1,2,3 = COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VS Static Negative Voltage	V_{SN}		-	-8.8	-	V

4.7 VDD5 Output

Table 4-7 VDD5 Output

(T_A = 25C， VCC = 15V, VBB = VBS1,2,3 = 12V, VS1,2,3 = COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VDD5 Output Voltage	V_{VDD5}		-	5	-	V
VDD5 Output	I_{VDD5}		-	30	-	mA

4.8 VBB Output

Table 4-8 VBB Output

(T_A = 25C， VCC = 15V, VBB = VBS1,2,3 = 12V, VS1,2,3 = COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VBB Output Voltage	V_{VBB}		-	12	-	V
VBB Output	I_{VBB}		-	30	-	mA

4.9 High-side/Low-side Output

Table 4-9 High-side/Low-side Output

(T_A = 25C， VCC = 15V, VBB = VBS1,2,3 = 12V, VS1,2,3 = COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High-side Output Voltage	V_{OH}	I_O = 20mA	-	0.2	-	V
Low-side Output Voltage	V_{OL}	I_O = 20mA	-	0.2	-	V
High-level Output Short-circuit Pulsed Current	I_{OH}	V_O = 0V	-	0.6	-	A
Low-level Output Short-circuit Pulsed Current	I_{OL}	V_O = 12V	-	0.6	-	A

4.10 Time Parameters

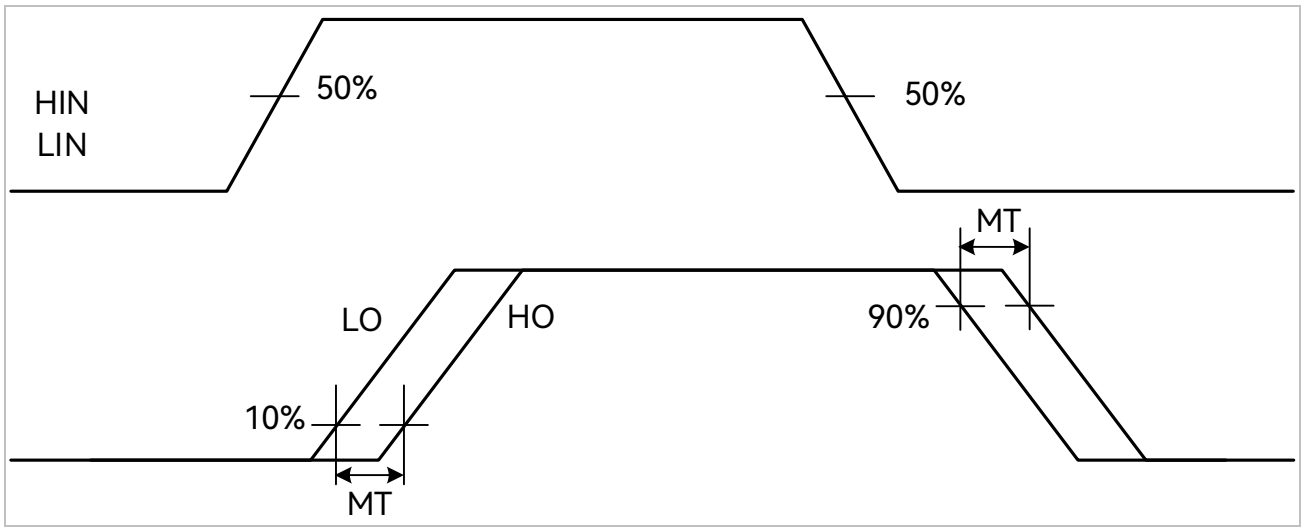
Table 4-10 Time Parameters

(T_A = 25C， VCC = 15V, VBB = VBS1,2,3 = 12V, VS1,2,3 = COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Propagation Delay	t_{on}		-	50	-	ns
Turn-off Propagation Delay	t_{off}		-	55	-	ns
Turn-on Rise Time	t_r	C_L = 1000pF	-	50	-	ns
Turn-off Fall Time	t_f	C_L = 1000pF	-	30	-	ns
Deadtime	DT		-	100	-	ns
High-low Side Delay Matching	MT		-	0	-	ns

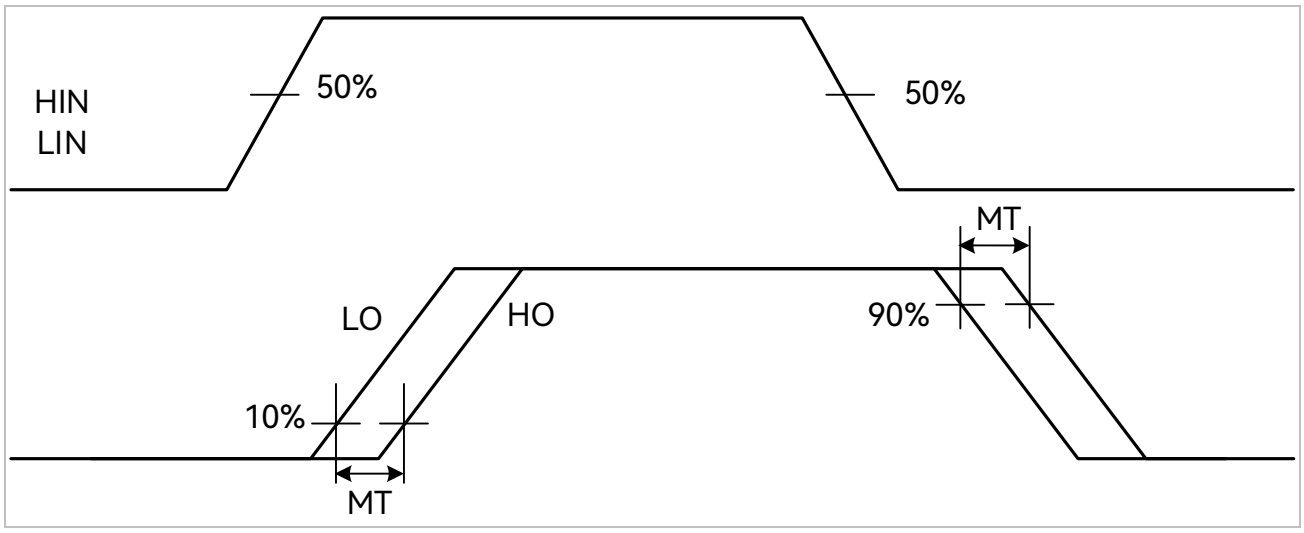
5 Propagation Delay Test Standards

Figure 5-1 Propagation Delay Test Standards



6 Propagation Delay Matching Test Standards

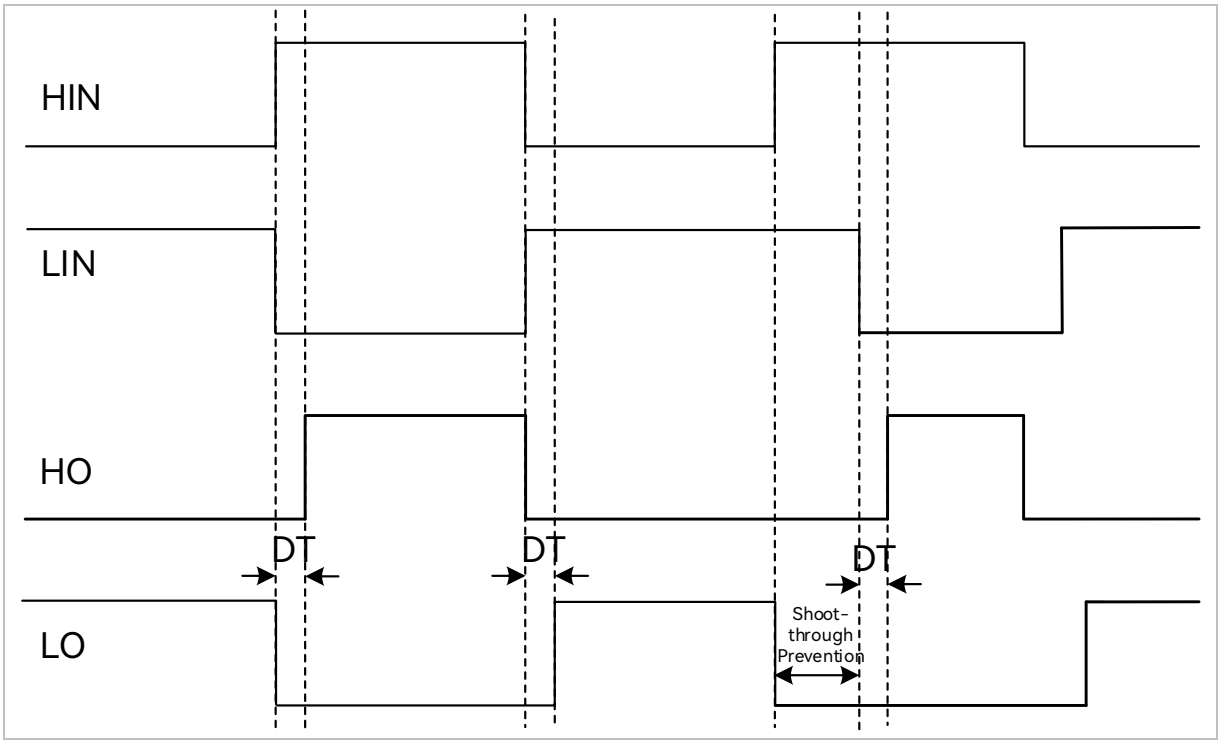
Figure 6-1 Propagation Delay Matching Test Standards



7 Cross-conduction Prevention

A protection circuit is specially designed inside the chip to enable cross-conduction prevention feature, which effectively prevents MOSFETs from damage when high-side and low-side input signals are interfered. Tube short-circuit failure. The figure below shows how the protection circuit works.

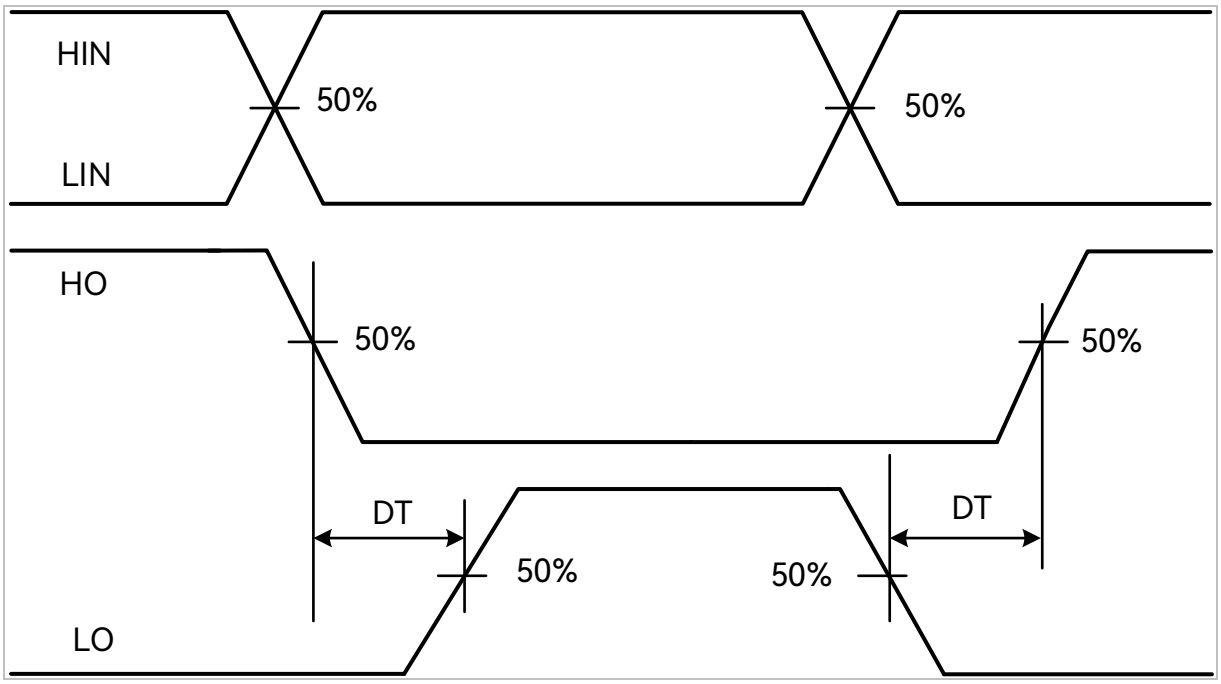
Figure 7-1 Schematic Diagram of Cross-conduction Prevention



8 Deadtime

The chip is designed with dedicated deadtime protection circuit. Both the high-side and low-side outputs are set to LOW during the deadtime. This feature prevents both MOSFETs of each half-bridge from switching on at the same time.

Figure 8-1 Deadtime Protection



9 Revision History

Rev.	Description	Date	Prepared By
V0.3	First release, preliminary datasheet	2025/06/04	Freya Fu

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